UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,841,822 B2
DATED : January 11, 2005
INVENTOR(S) : Violette

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete Title page illustrating figure, and substitute therefor new Title page illustrating figure (attached).

Delete drawing sheets 5-7, and substitute therefor drawing sheets 5-7, with the attached sheets.

Column 9,
Line 1, please delete "tor" before "having" and insert -- ter --.
Line 3, please delete "pulldown" after "second" and insert -- pullup --.

Signed and Sealed this

Twenty-seventh Day of September, 2005

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Violette

(10) **Patent No.: US 6,841,822 B2**
(45) **Date of Patent: Jan. 11, 2005**

(54) **STATIC RANDOM ACCESS MEMORY CELLS**

(75) Inventor: **Michael P. Violette, Boise, ID (US)**

(73) Assignee: **Micron Technology, Inc., Boise, ID (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/801,334**

(22) Filed: **Mar. 15, 2004**

(65) **Prior Publication Data**

US 2004/0173841 A1 Sep. 9, 2004

Related U.S. Application Data

(62) Division of application No. 10/300,175, filed on Nov. 19, 2002, now Pat. No. 6,753,581, which is a division of application No. 09/565,429, filed on May 5, 2000, now Pat. No. 6,750,107, which is a continuation of application No. 08/960,875, filed on Oct. 30, 1997, now Pat. No. 6,103,579, which is a continuation of application No. 08/819,546, filed on Mar. 17, 1997, now abandoned, which is a continuation of application No. 08/594,747, filed on Jan. 31, 1996, now abandoned.

(51) **Int. Cl.**[7] **H01L 29/788**

(52) **U.S. Cl.** **257/315**; 257/274; 257/314; 257/316; 257/338

(58) **Field of Search** 257/274, 314, 257/315, 316, 338; 365/200

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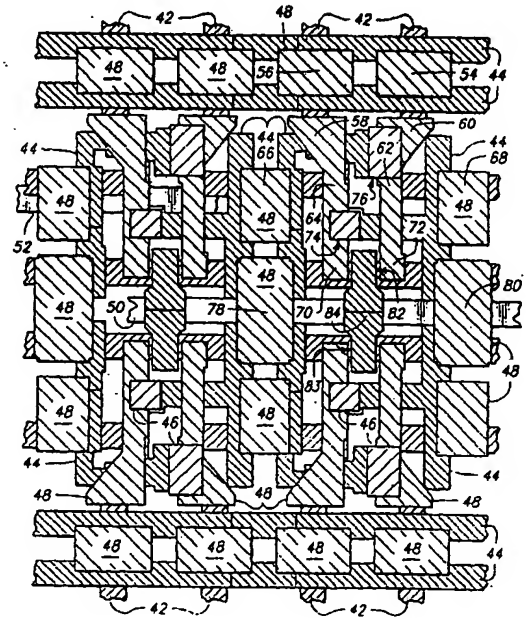
(57) **ABSTRACT**

A static random access memory cell comprising a first invertor including a first p-channel pullup transistor, and a first n-channel pulldown transistor in series with the first p-channel pullup transistor; a second invertor including a second p-channel pullup transistor, and a second n-channel pulldown transistor in series with the second n-channel pullup transistor, the first invertor being cross-coupled with the second invertor, the first and second pullup transistors sharing a common active area; a first access transistor having an active terminal connected to the first invertor; a second access transistor having an active terminal connected to the second invertor; and an isolator isolating the first pullup transistor from the second pullup transistor.

11 Claims, 7 Drawing Sheets



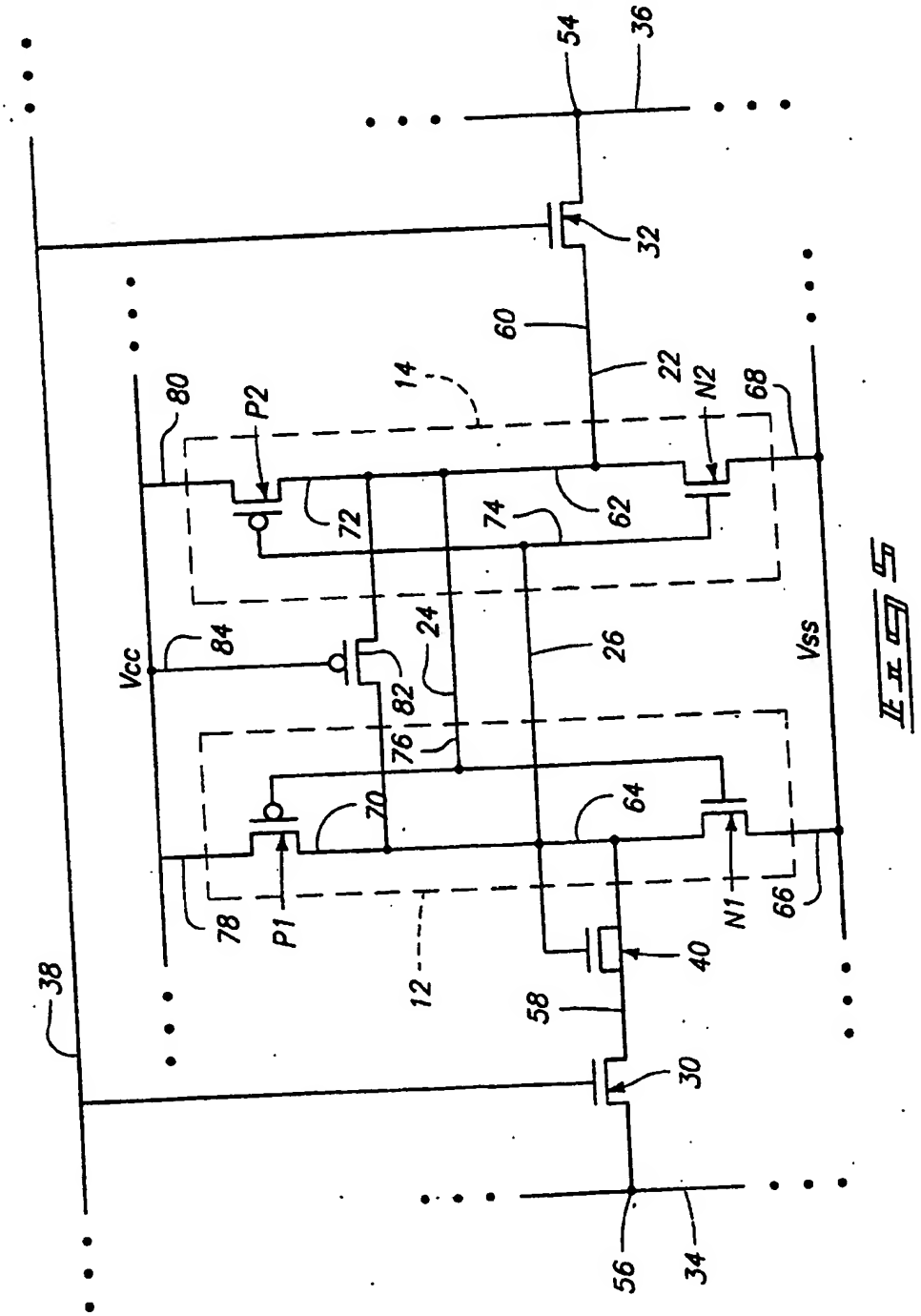

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FIG 5

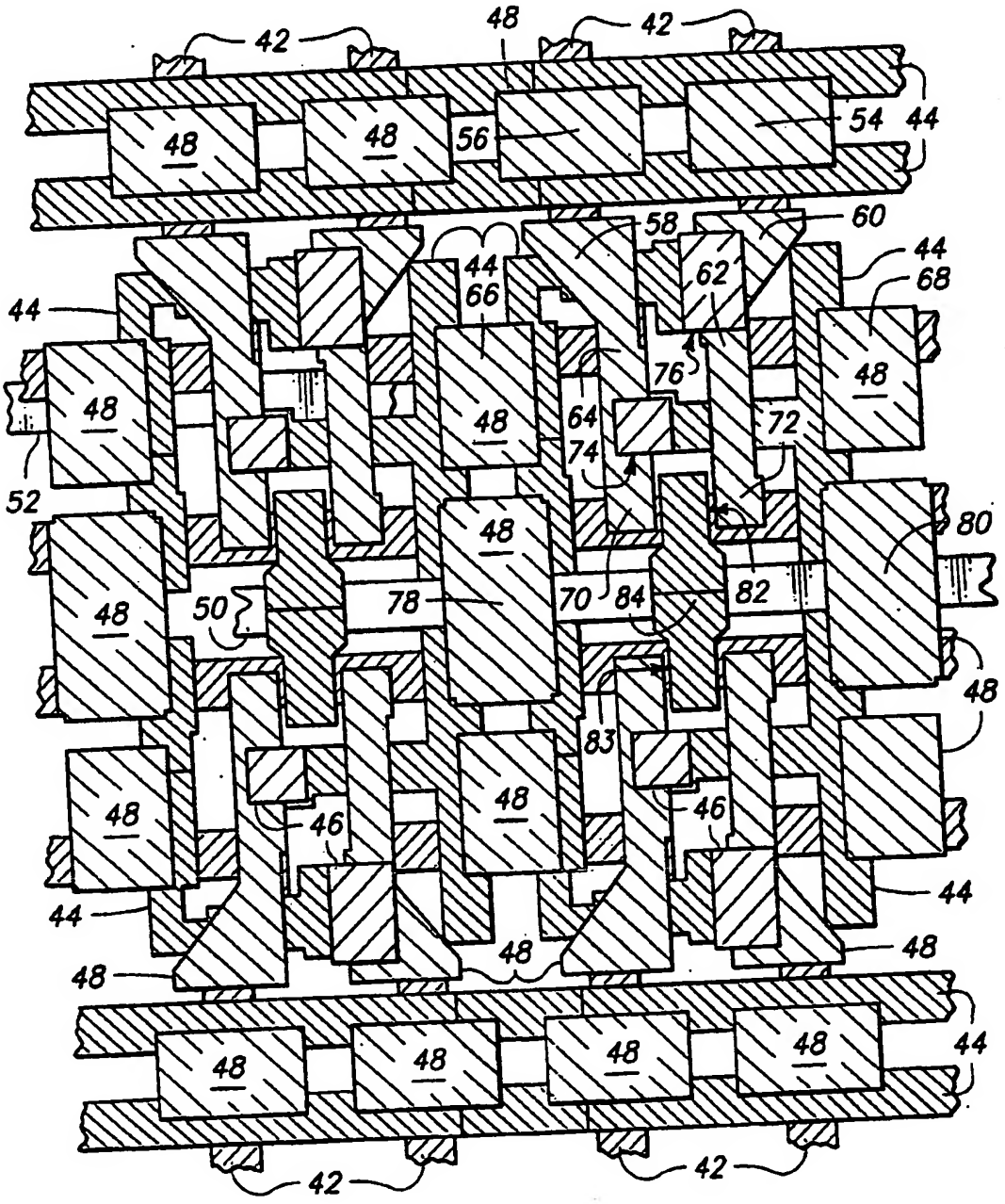
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Fig 6

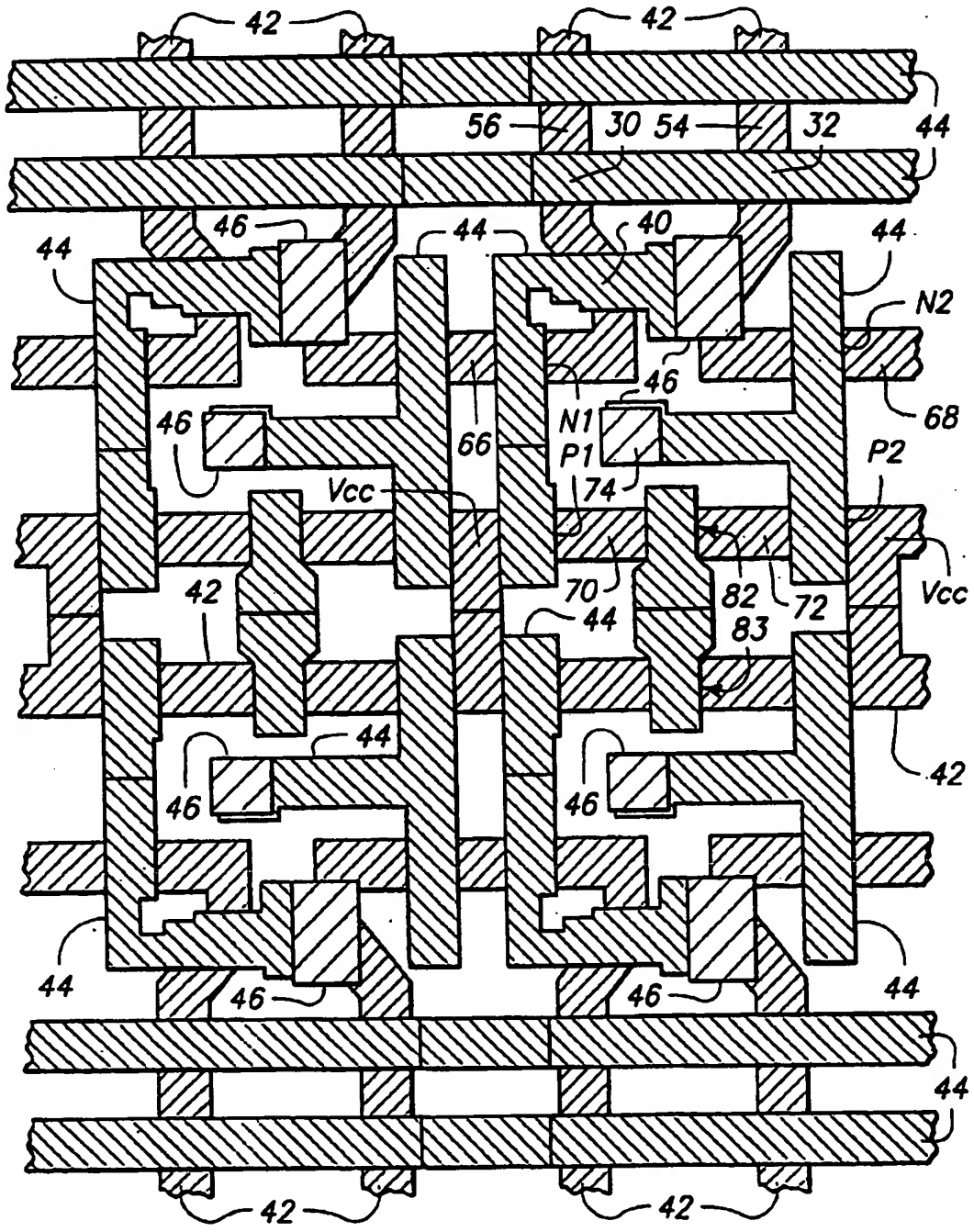
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Fig 7